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14. ABSTRACT
In this period of performance, we have tested the RF front-end, and characterized gain, phase, and delay linearity over the bandwidth of the transceiver, for both transmit and receive chain. We have manufactured and tested the ADC board, it is now functional. We have extended the time offset estimation algorithm to multi-tap channels (excluding Doppler). We are designing a final demonstration using the synchronization transceiver and in-house radar- and high-precision GPS hardware.

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Intelligent Automation Incorporated

Coherent distributed radar for high-resolution through-wall imaging

SBIR Phase I Progress Report 8

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Sponsored by

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Summary

In this period of performance, we have tested the RF front-end, and characterized gain, phase, and delay linearity over the bandwidth of the transceiver, for both transmit and receive chain. We have manufactured and tested the ADC board, it is now functional. We have extended the time offset estimation algorithm to multi-tap channels (excluding Doppler). We are designing a final demonstration using the synchronization transceiver and in-house radar- and high-precision GPS hardware.

1.0 INTRODUCTION

In this report we discuss progress in hardware design, synchronization algorithm, and definition of the final demonstration.

1.1 Synchronization algorithm

For time synchronization, we have completed Matlab simulations of our synchronization of multiple moving nodes, in a multi-tap multipath channel (excluding Doppler). The results indicate synchronization performance will likely be limited by hardware component performance, rather than achievable SNR, or the effects of mobility. We have also started implementation of the time offset estimation algorithm in the digital hardware. Finally, we have started to investigate if variations in the phase centers of the antennas could cause a bias in the timing measurement.

1.2 Hardware design

Part of the hardware design and implementation was supported by other efforts at IAI using the same hardware design. The RF layout has been sent out for manufacture, and has been tested. We have completed the ADC board redesign, manufacture and testing. The board functions well, other than a few dB of loss in the analog input circuit. We have tested the RF front-end and found that phase linearity is excellent of a 10-20MHz bandwidth. We also find a few dB of gain variation over the bandwidth, and a few ns of delay variation. We are now determining the stability of these parameters under temperature variations, between different hardware units, over time. We have started to determine how much these non-linearities may affect the synchronization accuracy, particularly in synchronization bias.

1.3 Preparation for final demonstration

We have accelerated the preparation of the final demonstration. We have selected the high precision GPS hardware and are designing two tripod-mounted platforms with the GPS hardware, and digital compasses. This will allow us to locate the radar antennas to within a few mm for stationary setups, and about 2cm for slow-moving setups. We are redesigning a previously developed through-wall radar to be interfaced to our synchronization hardware, and planning on having two or more units manufactured.

3.0 CONCLUSIONS AND WORK PLANNED FOR NEXT REPORTING PERIOD

The next reporting period will focus on implementation of the time offset estimation algorithm in the digital hardware, characterization and testing of the RF hardware, specifically the achieved noise figure, and ability to accurately measure hardware delays. We will complete the definition of the final demonstration and present a schedule of activities remaining in preparation for the demonstration.

3.0 REFERENCES

None.

4.0 LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS